

FPGArt

Painting with an FPGA

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What we learned...

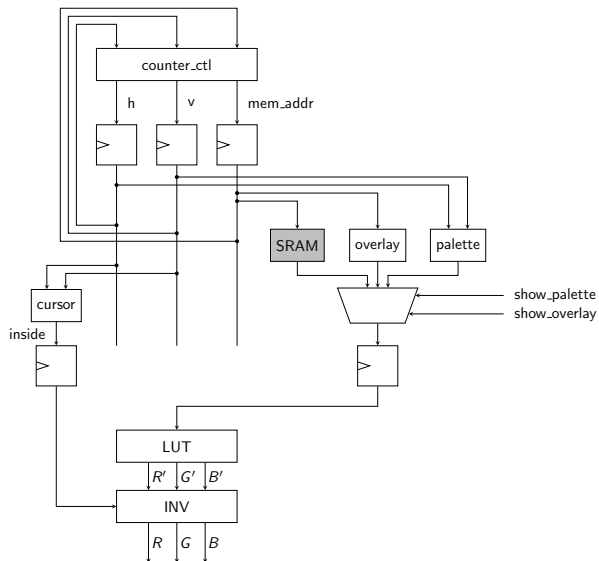
Statistics

Demo

Task

- ▶ Create a painting application on an FPGA
- ▶ Use a PS/2 Mouse for input and VGA for output
- ▶ Implement it completely in hardware (no softcore processor)

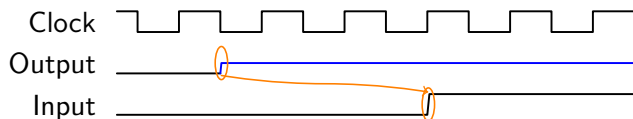
Graphic pipeline



Real hardware

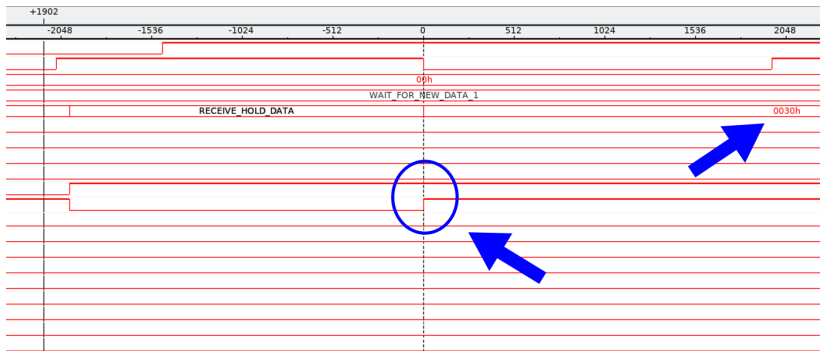
Working with real hardware discloses real world problems...

The pull-up resistor on the board is not fast enough for pulling the PS/2 clock lane up in one cycle at 40 MHz.



Hazards happen

Hazards happen – so better buffer all input signals...



FSM fed by an unbuffered input signal, behaving unpredictable (being in two states at the same time).

Statistics (without overlay)

| | |
|-------------------------------------|-----------------------------|
| Family: | Cyclone II |
| Device: | EP2C35F672C6 |
| Total logic elements: | 1,690 / 33,216 (5 %) |
| Total combinational functions: | 1,683 / 33,216 (5 %) |
| Dedicated logic registers: | 225 / 33,216 (< 1 %) |
| Total registers: | 225 |
| Total pins: | 99 / 475 (21 %) |
| Total memory bits: | 0 / 483,840 (0 %) |
| Embedded Multiplier 9-bit elements: | 4 / 70 (6 %) |
| Total PLLs: | 1 / 4 (25 %) |

Statistics (with overlay)

| | |
|-------------------------------------|------------------------------|
| Family: | Cyclone II |
| Device: | EP2C35F672C6 |
| Total logic elements: | 4,634 / 33,216 (14 %) |
| Total combinational functions: | 4,626 / 33,216 (14 %) |
| Dedicated logic registers: | 225 / 33,216 (< 1 %) |
| Total registers: | 225 |
| Total pins: | 99 / 475 (21 %) |
| Total memory bits: | 0 / 483,840 (0 %) |
| Embedded Multiplier 9-bit elements: | 4 / 70 (6 %) |
| Total PLLs: | 1 / 4 (25 %) |

DEMO